

## Analysis of PWM Inverter Fed Induction Motor Drive Based On Dead-Time Effect

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### Abstract

This paper will represent a dead time elimination scheme for sinusoidal pulse width modulation controlled inverter. Dead-time is necessary to prevent the short circuit of the power supply in PWM Inverters or converters. But, it will result in output voltage deviations and in case of lower values of current, lower order harmonics will be taken into account. So, dead time elimination is required in PWM Inverters or converters. To compensate the effect, two simple methods, which are adequate for sinusoidal pulse width modulation, helps in improving the of output voltage and reduces the harmonic distortion.

**Index terms:** Dead time elimination, sinusoidal pulse width modulation, harmonic optimization.

### I. Introduction

As per the types of dc sources, inverters are usually divided into VSIs and CSIs .considering the cost and performance, VSIs are usually prefer in real applications .It is well known that atypical semiconducting device used in inverter has an inbuilt delay time when it receives a signal from gate to start up its switching action.

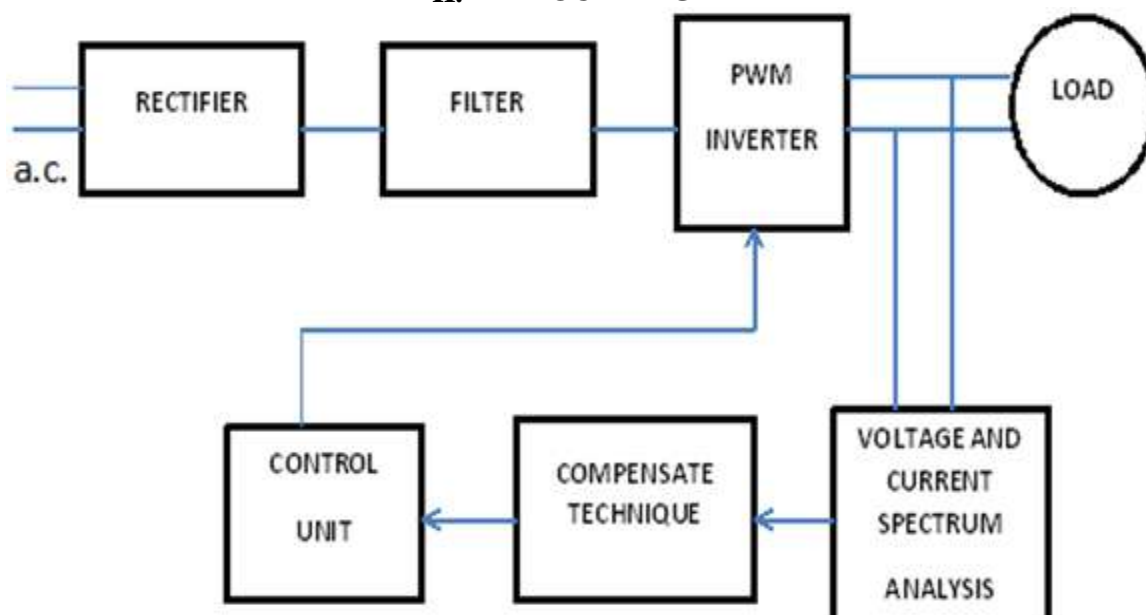
In inverter, the finite-turn off time may cause short circuit of the dc link at the instant of switchover between the two elements connected in series across the dc link. Thus it is essential to insert a time delay

in control signals to avoid the conduction overlap of the elements.

The state of the art in motor control provides an adjustable voltage and frequency to the terminals of the motor through a pulse width modulated (PWM) voltage source inverter drive. As the power devices change switching states, a dead time exists.

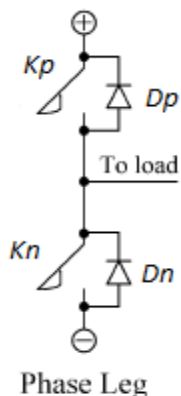
To avoid shoot-through in PWM controlled voltage source Inverters (VSI), dead-time, a small interval during which both the upper and lower switches in a phase leg are off, is introduced into the control of the standard VSI phase leg.

### II. BLOCKDIAGRAM



### III. Principle Of Dead-Time Elimination:

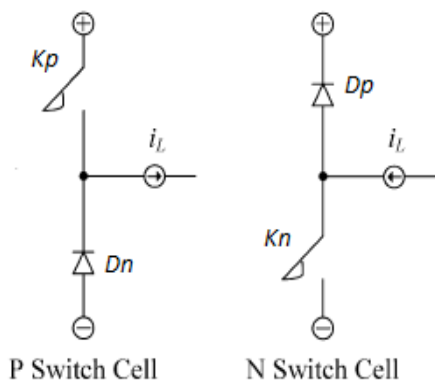
To explain the principle of the proposed dead-time elimination method, we refer to a generic phase leg of VSI, as shown in figure



A Generic Phase Leg of VSIs

Assuming the output current flows out of the phase leg, in each switching cycle, the current comes out from the upper device when  $Kp$  is on and freewheels through diode  $Dn$  when  $Kp$  is off. Here this current direction is defined as positive. Under this condition, the generic phase leg can be equivalently expressed as a P type switching cell shown in the figure. Similarly when load current flows into the phase leg, defined as negative, the current goes into the lower device when  $Kn$  is on and freewheels through diode  $Dp$  when  $Kn$  is off.

Under this condition, the generic phase leg can be equivalently expressed as a N type switching cell shown in the right figure. Actually a generic phase leg is a combination of one P switch cell and one N switch cell. There is no question that dead-time is not required for either a P switch cell or a N switch cell because both cells are configured with controllable switch in series with a uncontrollable diode.

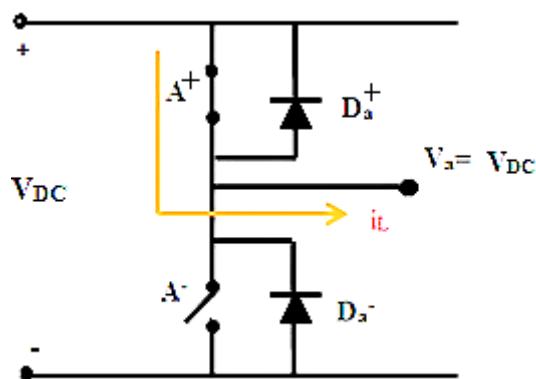


Equivalent switch cells.

When ac induction motors are operated using open-loop adjustable frequency drives, system instabilities may occur for certain frequency ranges and loading conditions. The cause of these instabilities can be inherent low-frequency motor instabilities, instability due to the interaction between the motor and the PWM inverter.

When the ac induction motor is fed by the voltage source inverter, the applied stator voltage waveforms contain harmonics generated by the PWM algorithm. The system stability will be affected by these harmonics, especially at low frequencies and no load conditions, causing additional machine losses and reduced efficiency.

### IV. EFFECT OF DEAD TIME



The effects of the dead time on the output voltage, can be examined from one phase of the PWM inverter. It consists of upper and lower power devices  $A^+$  and  $A^-$ , and reverse recovery diodes  $D_{a^+}$  and  $D_{a^-}$ , connected between the positive and negative rails of the power supply. Commutation of the power devices comes from the PWM generator. Output terminal  $V_a$  is connected to motor phase  $V_a$  and the current  $i_L$  is positive with respect to the motor. Examining the power device switching sequence as  $A^+$  is turning OFF and  $A^-$  turning ON, or  $A^-$  is turning OFF and  $A^+$  turning ON, there exists a time when both power devices cease to conduct. During the dead time output  $V_a$  appears to be floating, but the current  $i_L$  must conduct through reverse recovery diodes  $D_{a^+}$  and  $D_{a^-}$ . Depending on the current polarity, the reference voltage may be delayed by the dead time.

Possible commutation sequences:

In the first condition, the current  $i_L$  is positive.  $A^+$  transitions from ON to OFF and  $A^-$  from OFF to ON. During the dead zone,  $D_{a^-}$  conducts and  $D_{a^+}$  blocks the flow of current to the positive rail. This condition results in the correct voltage applied to the motor terminals.

In the second condition, the current  $i_L$  is positive.  $A^+$  transitions from OFF to ON and  $A^-$  from

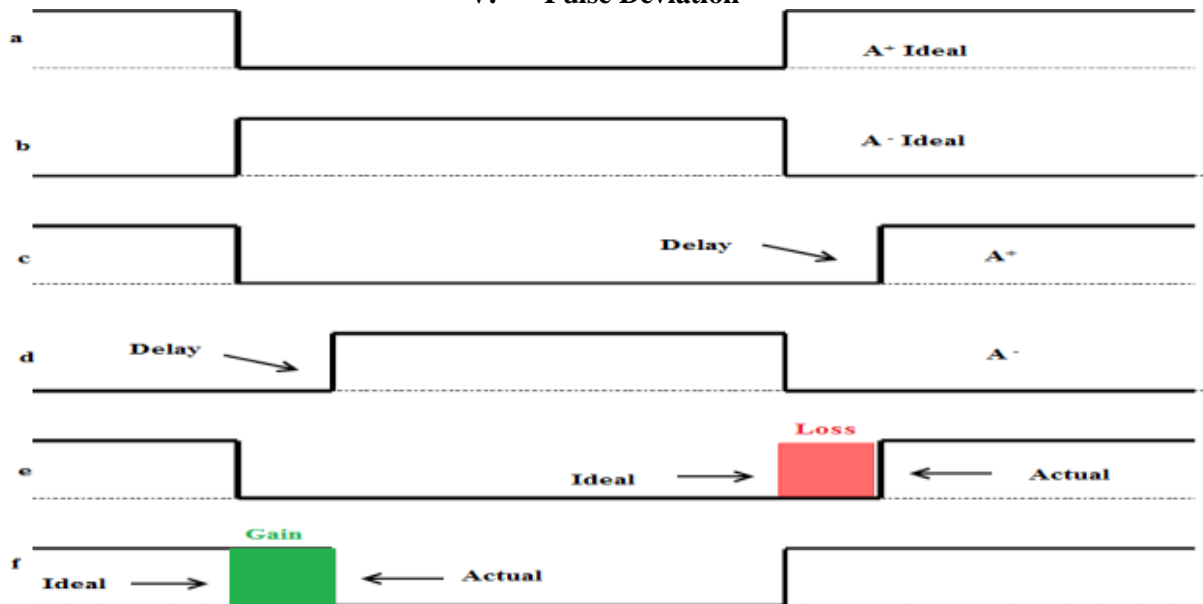
ON to OFF. During the dead zone, Da- continues conduction and Da+ blocks the flow of current to the positive rail. Current conducts in D2 until the dead time elapses, then A+ turns ON. This condition results in a loss of voltage at the motor terminals.

In the third condition, the current  $i_L$  is negative. A+ transitions from OFF to ON and A- from ON to OFF. During the dead zone, Da+ conducts and Da- blocks the current flow to the negative rail. This

condition results in the correct voltage applied to the motor terminals.

For the fourth condition, the current  $i_L$  is negative. A+ transitions from ON to OFF and A- from OFF to ON. During the dead zone, Da+ continues conduction and Da- blocks the flow of current to the negative rail. Current conducts in D1 until the dead time elapses, then A- turns ON. This condition results in a gain of voltage at the motor terminals.

## V. Pulse Deviation



Trace 3a and 3b are the ideal pulse times; if applied, the resulting fundamental voltage would be of the correct magnitude and phase.

In trace 3c, A+ transitions from ON to OFF, but there must be a delay time before A- in trace d can turn from OFF to ON. Likewise as A- in trace 3d transitions from ON to OFF, A+ in trace 3c must delay before it can turn on.

Consider  $i_L$  positive in trace 3e, as A+ transitions from ON to OFF, there is no reduction or gain to the pulse time as compared to the ideal pulse time. As A+ transitions from OFF to ON, the pulse time decreases from the ideal resulting in a deviation to the pulse time and an incorrect fundamental voltage to the load.

When  $i_L$  is negative as in trace 3f, A+ is held on longer than the ideal, resulting in an increase in pulse time, and an incorrect fundamental voltage applied to the load. As A+ transition from OFF to ON, there is no reduction or gain to the pulse as compared to the ideal pulse.

## VI. Future scope

Reduction in harmonic distortion at variable loading condition.

Efficiency improvement using delay model

## VII. Conclusions

Total Harmonic Distortion (THD) was reduced and simulation result with and without compensation techniques are compared for justification.

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